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(30) Priority:	25.02.8723.04.87 JPJP 62 4034362100287	(71) Applicant: NEC CORP
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(54) HARDWARE LOGICAL  
SIMULATOR

(57) Abstract:

**PURPOSE:** To easily detect the coverage of simulation by writing and reading prescribed data in and out of an address of a storage means determined according to the state of a specified signal group after variation at the time of simulation.

**CONSTITUTION:** A specifying means 2 which specifies a signal group in a simulation model and an incorporating means 3 which generates a storage means inputting the specified signal group as an address and incorporates it in the model are provided. Further, a writing means 1 which writes the prescribed data in the address of the storage means determined according to the state of the state of the signal group specified by the specifying means 2 after the variation at the end of simulation and a reading means 5 which reads the stored data are provided. The storage data in the storage means are checked after the end of the simulation and its unwritten address shows a combination where simulation is not performed. Consequently, the combination where no simulation is performed is regarded as a target, a repeated test case is eliminated, and efficient simulation for sufficient logical verification becomes possible.

